CLAIM AMENDMENTS

Claim Amendment Summary

Claims pending

- Before this Amendment: Claims 1-18, 20-26, and 28-39
- After this Amendment: Claims 1-18, 20-26, and 28-39

Non-Elected, Canceled, or Withdrawn claims: None

Amended claims: None

New claims: None

Claims:

1. (Previously Presented) A method of internally controlling a clock signal of an integrated circuit device such that a data path of the integrated circuit device is initialized in a test mode, comprising the steps of:

upon a power-up condition in the test mode of the integrated circuit device forcing the clock signal of the integrated circuit device to a first logic state, thereby causing a master element of the integrated circuit device to load in first data and to conduct; and

upon completion of the power-up condition forcing the clock signal of the integrated circuit device to a second logic state, thereby latching in the first data to the master element and causing a slave element of the integrated

circuit device to load in second data generated by the master element and to conduct.

2. (Previously Presented) The method of claim 1, wherein the first logic state is a low logic state and the second logic state is a high logic state.

3. (Previously Presented) The method of claim 1, wherein the power-up condition of the integrated circuit device is controlled by a power-on-reset signal of the integrated circuit device.

4. (Previously Presented) The method of claim 3, wherein the power-on-reset signal is an internally generated signal which changes logic state once a threshold value of a positive power supply is passed as the positive power supply rises.

5. (Previously Presented) The method of claim 1, wherein the clock signal of the integrated circuit device is an external clock signal of the integrated circuit device or a derivative signal of the external clock signal.

6. (Previously Presented) The method of claim 1, wherein the master element of the integrated circuit device is a master latch element and the slave element is a slave latch element.

7. (Previously Presented) The method of claim 1, wherein the master element of the integrated circuit device is a master flip-flop element and the slave element is a slave flip-flop element.

8. (Previously Presented) The method of claim 1, wherein upon the power-up condition of the integrated circuit device, the clock signal is internally clocked.

9. (Previously Presented) The method of claim 1, wherein when the master element is conducting the slave element does not conduct and when the slave element is conducting the master element does not conduct.

10. (Previously Presented) The method of claim 1, wherein the test mode is entered upon the power-up condition of the integrated circuit device.

11. (Previously Presented) The method of claim 1, wherein the data path is an address path.

12. (Previously Presented) The method of claim 1, wherein in the test mode the integrated circuit device is tested at a voltage above a normal operating voltage of the integrated circuit device.

13. (Previously Presented) The method of claim 12, wherein the clock signal is tested in both the first logic state and the second logic state at the voltage.

14. (Previously Presented) The method of claim 1, wherein the integrated circuit device is a synchronous clocked device.

15. (Previously Presented) The method of claim 1, wherein conduction of the master element and conduction of the slave element initializes an address path of the integrated circuit device such that a plurality of columns and a plurality of rows of the integrated circuit device are not selected.

16. (Previously Presented) The method of claim 1, wherein conduction of the master element and conduction of the slave element initializes an address path of the integrated circuit device such that a plurality of columns and a plurality of rows of the integrated circuit device are selected.

17. (Previously Presented) The method of claim 16, wherein a plurality of bitlines true of the integrated circuit device are held at a first voltage level and a plurality of bitlines complement of the integrated circuit device are held at a second voltage level.

18. (Previously Presented) A method, comprising:

providing power to an integrated circuit;

loading a first data bit into a master latch and causing the integrated circuit to enter a test mode before the power attains a predetermined level, the master latch being disposed on the integrated circuit;

generating a second data bit from the first data bit;

latching the first data bit in the master latch; and

loading the second data bit into a slave latch that is disposed on the integrated circuit.

19. (Canceled)

20. (Previously Presented) The method of claim 18 wherein generating the second data bit comprises generating the second data bit equal to the first data bit.

21. (Previously Presented) The method of claim 18 wherein generating the second data bit comprises generating the second data bit equal to a complement of the first data bit.

22. (Previously Presented) The method of claim 18 wherein generating the second data bit comprises generating the second data bit before and after the power attains the predetermined level.

23. (Previously Presented) The method of claim 18 wherein:

loading the first data bit into the master latch comprises simulating an external clock signal having a first clock state; and

latching the first data bit in the master latch and loading the second data bit into the slave latch comprise simulating the external clock signal having a second clock state.

24. (Previously Presented) The method of claim 18 wherein:

loading the first data bit into the master latch comprises simulating an external clock signal inside the integrated circuit, the clock signal having a first clock state; and

latching the first data bit in the master latch and loading the second data bit into the slave latch comprise simulating the clock signal having a second clock state.

25. (Previously Presented) A method, comprising:

generating a power-on reset signal having a first reset state when power supplied to an integrated circuit has a predetermined first level causing the integrated circuit to enter a test mode;

generating the power-on reset signal having a second reset state when the power has a second predetermined level;

loading a first data bit into a master latch of the integrated circuit in response to the power-on reset signal having the first state;

generating a second data bit from the first data bit;

storing the first data bit in the master latch in response to the power-on reset signal having the second state; and

loading the second data bit into a slave latch of the integrated circuit in response to the power-on reset signal having the second state.

26. (Previously Presented) The method of claim 25 wherein:

generating the power-on reset signal having the first state comprises generating the power-on reset signal having the first state when an integrated-circuit supply voltage has a first predetermined voltage level; and

generating the power-on reset signal having the second state comprises generating the power-on reset signal having the second state when the supply voltage has a second predetermined voltage level.

27. (Canceled)

28. (Previously Presented) The method of claim 25 wherein generating the second data bit comprises generating the second data bit in response to the power-on reset signal having either the first state or the second state.

29. (Previously Presented) The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating a test signal having a first test state.

30. (Previously Presented) The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating multiple test signals each having a first test state.

31. (Previously Presented) The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise:

generating a test signal having a test state; and

simulating an external clock signal having a clock state in response to the test signal having the test state.

32. (Previously Presented) The method of claim 25 wherein:

loading the first data bit into the master latch comprises simulating an external clock signal having a first clock state in response to the power-on reset signal having the first reset state; and

storing the first data bit in the master latch and loading the second data bit into the slave latch comprise,

generating a test signal having a test state, and

simulating the clock signal having a second clock state in response to the test signal having the test state.

33. (Previously Presented) The method of claim 25 wherein:

loading the first data bit into the master latch comprises,

simulating an external clock signal having a first clock state in response to the power-on reset signal having the first reset state,

generating a test signal having a test state, and

generating the first data bit in response to the test signal; and

storing the first data bit in the master latch and loading the second data bit into the slave latch comprise simulating the clock signal having a second clock state in response to the power-on reset signal having the second reset state and the test signal having the test state.

34. (Previously Presented) The method of claim 25 wherein:

loading the first data bit into the master latch comprises,

simulating an external clock signal having a first clock state in response to the power-on reset signal having the first reset state,

generating a test signal having a first test state, and

generating the first data bit in response to the test signal; and

storing the first data bit in the master latch and loading the second data bit into the slave latch comprise,

generating the test signal having a second test state, and

simulating the clock signal having a second clock state in response to the power-on reset signal having the second reset state and the test signal having the second test state.

35. (Previously Presented) A method, comprising:

providing power to an integrated circuit;

loading a first data bit into a master latch and causing the integrated circuit to enter a test mode before the power attains a predetermined level, the master latch being disposed on the integrated circuit;

latching the first data bit in the master latch; and

loading the first data bit into a slave latch of the integrated circuit.

36. (Previously Presented) The method of claim 35 wherein:

loading the first data bit into the master latch comprises generating a clock signal having a first clock state; and

latching the first data bit in the master latch and loading the first data bit into the slave latch comprise generating the clock signal having a second clock state.

37. (Previously Presented) The method of claim 35 wherein:

loading the first data bit into the master latch comprises generating a clock signal inside the integrated circuit, the clock signal having a first clock state; and

latching the first data bit in the master latch and loading the first data bit into the slave latch comprise generating the clock signal having a second clock state.

38. (Previously Presented) The method of claim 18 wherein:

latching the first data bit comprises latching the first data bit in the master latch after powering up the integrated circuit; and

loading the second data bit comprises loading the second data bit into the slave latch when the power attains the predetermined level.

39. (Previously Presented) The method of claim 35 wherein:

latching the first data bit comprises latching the first data bit in the master latch when the power attains the predetermined level; and

loading the first data bit into the slave latch comprises loading the first data bit into the slave latch when the power attains the predetermined level.